Ultra-efficient design of robust RS flip-flop in nanoscale with energy dissipation study

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Abstract: By the gradual increasing of the attribute size and energy utilization in VLSI chips the component of energy depleted owing to information forfeiture in irreversible valuations will turn into a crucial drawback in the future. Nano components, particularly quantum-dot cellular automata (QCA), have attained extensive interests for their foremost aspects as contrasted to the typical complementary metal oxide semiconductor (CMOS) circuits. QCA, especially due to its substantial diminution in latency, dimension, and energy utilization of circuits, is counted as a latent substitute for the CMOS technology. In this study, a design of RS flip-flop circuit in QCA is proposed. We review an approach for simplified outline of QCA circuits such that the dimensions and energy depletion are substantively decreased. The designed circuit is carried out using single layer and does not involve any rotated cells which particularly expand the fabrication of the outline. The proposed design is simulated with QCADesigner and energy utilization is estimated using QCAPro tool which is a widespread simulation tool. Assessments specify that the outlined structure significantly reduces the number of cells, extent, and latency and depletes very low power which simplifies the complete circuit manufacture and implementation.

Keywords: quantum-dot cellular automata; RS flip-flop; QCADesigner; energy depletion; QCAPro

1. Introduction
In current years, because of the advent of crucial constrictions against substantial scalability of the complementary metal oxide semiconductor (CMOS) outline, several deficiencies and difficulties have
been classified. A few of these problems inherent to this outline are short channel influences and extreme leakage power utilization (Liu, Lu, O’Neill, & Swartzlander, 2014; Roohi, Khademolhosseini, Sayedsalehi, & Navi, 2014). A number of substitute technologies (Abdullah-Al-Shafi & Bahar, 2016a) as carbon nanotube field effect transistor, nanowire-based transistor and quantum-dot cellular automata (QCA) (Lent, Tougaw, Porod, & Bernstein, 1993) have previously been recommended for the CMOS outline to solve these shortcomings. Among the substitute resolutions, QCA has concerned far more consideration as it has presented particular device thickness, rapid operation and extremely low energy (Abdullah-Al-Shafi, 2016a; Abdullah-Al-Shafi & Bahar, 2016a; Islam, Shafi, & Bahar, 2016). In every QCA cell, two arrangements subsist that can program the binary information. The majority voter performs a considerable part in the circuits assembled based on the QCA technology (Abdullah-Al-Shafi, 2016a; Abdullah-Al-Shafi & Bahar, 2016a; Al Shafi, Bahar, & Islam, 2015; Islam, Shafi, & Bahar, 2015). With the inverter and majority voter permits manufacturers to form any functions in QCA technology (Abdullah-Al-Shafi, Aneek, & Bahar, 2017; Abdullah-Al-Shafi & Bahar, 2017; Abdullah-Al-Shafi, Bahar, Ahmad, & Ahmed, 2017; Abdullah-Al-Shafi, Bahar, Ahmad, Bhuiyan, & Ahmed, 2017; Abdullah-Al-Shafi et al., in press; Bahar, Uddin, Abdullah-Al-Shafi, Bhuiyan, & Ahmed, 2017; Biswas, Bahar, Habib, & Abdullah-Al-Shafi, 2017; Hassan et al., 2017). Energy utilization is certainly the foremost affair in current VLSI circuits. Because of the ever growing requirements for convenient electronic structures and the inconsistent progress of the semiconductor and battery production businesses, expanding the functioning time between every single battery charge has to turn into incredibly curtail. Moreover, the inconsistent scaling of the dimension of transistors and power source voltage has directed to several deficiencies (Abdullah-Al-Shafi, 2016a; Abdullah-Al-Shafi et al., 2017; Liu et al., 2014) forming hot spots in CMOS microchip. Accordingly, separate computational patterns through evolving nanotechnologies, concentrate on minimal power depletion and radically small extent should be measured. Landauer showed that each one bit of information forfeit in an irreversible assessment leads to $k_B T \ln 2$ joules depletion of heat energy, where $k_B$ is denoted as Boltzmann constant and $T$ is the room temperature (Landauer, 1961). Though the depletion of the existing CMOS circuits is far excessive than $k_B T \ln 2$, in the forthcoming with eventual scaling of attribute size and power utilization based on evolving technologies, this hypothetical constraint may turn into a main restriction (Sen, Dutta, Some, & Sikdar, 2014). In this study, an enhanced Reset Set (RS) flip-flop is presented, which in contrast with the former outlines involve the minimal number of QCA cells and extent. As well the proposed design depletes very low energy. The remainder of this study is prepared as follows: Section 2 concisely analyses the QCA fundamental properties. Section 3 illustrates the proposed QCA design. The simulation outcomes and assessments are organized in Section 4 and lastly, Section 5 deduces the study.

2. A concise study of the QCA technology

2.1. QCA fundamentals

Each four-sided QCA cell contains four quantum dots employed by a pair of electrons. Because of the coulomb revulsion concerning two electrons, they will be sited at transversely reverse places. The parameter $P$, presented by Equation (1), is described to determine this placement, where the value $\rho_i$ is the chance of the existence of an electron in quantum-dot $i$ (Tougaw & Lent, 1996).

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)}$$

(1)

Because of a higher inter-cell potential, the electrons cannot channel between two cells. Though they can channel between adjacent dots. There present two arrangements in every cell with the polarizations labeled as +1 and −1 which are signified by binary values of 1 and 0 (Tougaw & Lent, 1996). Once a bit switches from “0” to “1” and vice versa, no authentic charging and discharging of capacitors appear as in CMOS. Besides, conduction of logic from one cell to another is achieved by the interface of electrons in adjoining cells and there is no movement of current between QCA cells. Hence, there is no energy depletion through the state changeover and propagation in QCA. Thus, QCA depletes very little power as contrasted to the CMOS circuits. In QCA, a wire is comprised of an arrangement of QCA simple cells that circulates an input value to the target cell by the columbic
revulsions concerning the electrons of the successive cells. The wires are comprehended in two categories, including 45-degree or 90-degree cells (Abdullah-Al-Shafi, 2016a, 2016b; Abdullah-Al-Shafi & Bahar, 2016). The major QCA logic gates are the three input majority voters and inverter which are presented in Figure 1(b)–(d), correspondingly.

The arrangement of the inverter and majority voters specifies a comprehensive gate identified the minority gate. As per the type of the QCA formation, the circuits in QCA are generally devised based on the inverter and majority gates (Tougaw & Lent, 1994). A clock is necessary to provide the potential gain for cells and manage the data flow in QCA circuits. It is attained by scheming the potential block energies between adjoining quantum-dots. A four stage clocking arrangement is applied to specify the circulation of data over the logic circuits (Abdullah-Al-Shafi & Bahar, 2016a, 2016b). Specified a number of potential blocks, the energy stages can be outlined in four clocking regions with \( \pi/2 \) phase variance (Hennessy & Lent, 2001). This clocking structure containing switch, hold, release and relax periods is explained in Figure 2.

QCA Wire crossing can be realized by tree methodologies including coplanar and multi-layer (Shin, Jeon, & Yoo, 2013). In the first method, present in Figure 3(a), to transfer the accurate values in every single wire, multi-layer outline should be utilized. In this technique, a wire is applied in one layer and another wire is applied in a cross position in the other layer. The next method, presented in Figure 3(b), to transfer the accurate values in every single wire, a coplanar technique is applied. For this procedure, one of two wires is applied with 45-degree cells and the other wire is applied with 90-degree cells.

Figure 1. QCA logic (a) Cells indicating logic “0” and logic “1”, (b) Simple inverter, (c) QCA robust inverter and (d) Three-input majority voter.

Figure 2. Four clocking zones in QCA outline.
2.2 Stable values concern in QCA technology

There are usually two systems for recognizing the stable values essential in a QCA cell. First one is a QCA system that allocates the essential uniform polarization, whereas the second method, utilized the dot-level operation of cells inside the QCA circuit (Walus & Jullien, 2006).

The design of stable input driver in the QCA circuits on external inputs is presented in Figure 4. A separate extent must be counted to affect the values in the circuits. In practical circumstances, an extra space and supplementary arrangement and channeling over another level to distribute the preferred value into stable input cells are essential to insert arbitrary values into stable cells.

2.3 QCA circuits construction

QCA circuits can be constructed by several approaches comprising, semiconductor, molecular formations, nanomagnetic and metal-island. QCA semiconductor approach can be manufactured with electron beam lithographically outlined on the GaAs/ALGas heterostructure substance as presented in (Smith et al., 2003). The metal-island organization can be formulated on a silicon wafer. The formulation of a cell with aluminum metallic dots and expansions of this sort of QCA cell to a wire have been reviewed in (Orlov, Amlani, Bernstein, Lent, & Snider, 1997). Nanomagnetic QCA cell construction has been presented in (Cowburn & Welland, 2000). Assembly and presentation of a QCA cell on an ion-implanted phosphorus-doped silicon has been reported in (Mitic et al., 2006). Various constituents like graphene (Wang & Lieberman, 2004) can be used to realize the molecular method. It can be perceived in recent times that there is a notable possibility for improvement in the construction of QCA based nanocircuits.

Figure 3. QCA multi-layer wire crossing (a) and coplanar approach (b).
3. Proposed QCA circuit

The SR flip-flop is measured as one of the utmost elementary sequential logic circuits. This plain circuit is mainly a single-bit memory bistable design which has two fixed inputs, one that will “SET” the circuit and another that will “RESET” the circuit as presented in Figure 5.

The SR account stands for “Set-Reset”. The reset state resets the circuit back to its initial position with a result Q that will be either at a logic stage “0” or logic “1” rest on this set/reset state.

The majority gate illustration of the proposed circuit is presented in Figure 6(a) and the equation is given to as follows.

$$Q_{n'} = mv(S, R, Q_n)$$  \hspace{1cm} (2)

The QCA presentation of the proposed circuit is shown in Figure 6(b) where R and S are the input and Q, and Q denoted as output. The central loop of the circuit has single delay; however, at the output, Q is accessible 2.75 clocking levels after R and S have been affected. The proposed layout is confirmed with QCADesigner ver. 2.0.3, with the succeeding factors for a bistable approximation: Cell size = 18 nm, Number of samples = 20,000, Radius of effect = 90 nm, Clock high = 9.8e-22 J, Clock low = 3.8e−23 J, Clock amplitude factor = 2, Relative permittivity = 12.90, Layer separation = 11.5 nm, Maximum Iterations per sample = 100 and Convergence tolerance = 0.001. For coherence vector simulation the succeeding factors are: Temperature = 1.00 K, Relaxation time = 1.0e-15 s, Time step = 1.0e-16 s, Overall simulation time = 7e−11 s, Clock shift = 0, Radius of effect = 80 nm, Clock low = 3.8e−23 J, Clock amplitude factor = 2 and Relative permittivity = 12.90.

4. Results study and assessments

This section, the outlined circuit is simulated with the QCADesigner tool (Walus, Dysart, Jullien, & Budiman, 2004). Simulation result of the flip-flop is shown in figure 7 and from the result, it is clear that the result is attained after 2.75 delay. The delay is indicated with a blue arrow.

The outlined circuit is attained with 2 fixed inputs, 1 majority gate, 14 cells with extent of 0.01 \( \mu \text{m}^2 \) and 4 clocking zones that is considerably enriched than existing layout.
4.1. Evaluation of proposed and previous RS flip flop

The evaluation is accomplished in terms of the number of applied cells, clock phase, and used space (Abdullah-Al-Shafi & Bahar, 2017; Abdullah-Al-Shafi et al., 2017). The layout in (Vetteth, Walus, & Dimitrov, 2003) consumes 76 QCA cell with a dimension of 0.09 μm² and latency 6. Proposed flip-flop acquired an improvement of 81.58, 88.89 and 54.17% in terms of used cell, extent and delay, correspondingly. As well the proposed circuit do not use any rotated cell.

Comparing with (Rezaei, 2017), the outlined circuit attained an enhancement of 46.16, 58.33, and 45.00%, respectively. In the same way, other estimation is organized in Table 1 and improvement analysis with earlier flip-flop is shown in Figure 8.

4.2. Energy depletion of the proposed layout

The energy depletion by QCA cell is considered with the higher bound energy dissipation pattern is given as

\[
P_{\text{diss}} = \frac{E_{\text{diss}}}{T_{\text{cc}}} \left[ -\frac{\Gamma^+}{|\Gamma^+|} \tanh \left( \frac{h|\Gamma^+|}{K_c T} \right) + \frac{\Gamma^-}{|\Gamma^-|} \tanh \left( \frac{h|\Gamma^-|}{K_c T} \right) \right]
\]

(3)

To estimate the energy depletion of outlined circuit, we used QCAPro (Srivastava, Asthana, Bhanja, & Sarkar, 2011). The consumption is determined in several tunneling energy stages at 2 K temperature, presented in Table 2. Moreover, the average switching energy, average leakage energy and average energy depletion at three different tunneling energy stages of outlined circuit are shown in Figure 9.

<table>
<thead>
<tr>
<th>RS flip-flop</th>
<th>Layout</th>
<th>Cell number</th>
<th>Area (μm²)</th>
<th>Delay</th>
<th>Rotated cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS -1</td>
<td>In Vetteth et al. (2003)</td>
<td>76</td>
<td>0.09</td>
<td>6</td>
<td>Yes</td>
</tr>
<tr>
<td>RS -2</td>
<td>In Huang, Momennzadeh, and Lombardi (2007)</td>
<td>66</td>
<td>0.08</td>
<td>7</td>
<td>No</td>
</tr>
<tr>
<td>RS -3</td>
<td>In Jagarlamudi, Saha, and Jagarlamudi (2011)</td>
<td>60</td>
<td>0.07</td>
<td>6</td>
<td>Yes</td>
</tr>
<tr>
<td>RS -4</td>
<td>In Choi (2005)</td>
<td>33</td>
<td>0.04</td>
<td>5</td>
<td>No</td>
</tr>
<tr>
<td>RS -5</td>
<td>In Rezaei (2017)</td>
<td>26</td>
<td>0.024</td>
<td>5</td>
<td>No</td>
</tr>
<tr>
<td>RS -6</td>
<td>In Dutta and Mukhopadhyay (2014)</td>
<td>18</td>
<td>0.02</td>
<td>3.75</td>
<td>No</td>
</tr>
<tr>
<td>Proposed</td>
<td></td>
<td>14</td>
<td>0.01</td>
<td>2.75</td>
<td>No</td>
</tr>
</tbody>
</table>
Figure 8. An improvement study of outlined flip flop with previous layouts.

Table 2. Energy depletion study of proposed RS Flip-flop

<table>
<thead>
<tr>
<th>Design</th>
<th>Avg. leakage energy</th>
<th>Avg. switching energy</th>
<th>Avg energy depletion</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Avg. E&lt;sub&gt;k&lt;/sub&gt;</td>
<td>1.0 E&lt;sub&gt;k&lt;/sub&gt;</td>
<td>1.5 E&lt;sub&gt;k&lt;/sub&gt;</td>
</tr>
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<td></td>
<td>4.32</td>
<td>12.38</td>
<td>21.44</td>
</tr>
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<td></td>
<td>17.9</td>
<td>15.2</td>
<td>12.85</td>
</tr>
<tr>
<td></td>
<td>22.22</td>
<td>27.58</td>
<td>34.29</td>
</tr>
</tbody>
</table>

Figure 9. (a) Average leakage energy, switching energy and total energy depletion at three distinctive tunneling energy (T = 2.0 K) levels and (b) Energy depletion map for the outlined QCA circuit at 2 K temperature with 1.5 E<sub>k</sub>.
4.3. Consistency of the proposed circuit

The average output polarization (AOP) of the circuit is lessened by rising the temperature (Hassan et al., 2017). The temperature consequence on the AOP of the outlined circuit is shown in Figure 10. The AOP of the RS flip-flop is steadily lessened, up to a temperature of \( T = 6 \text{ K} \). Hence, in between 1 and 6 K, the proposed circuit functions competently. Beyond that temperature the AOP is depleted, and the circuit break downs. To assemble the AOP at several temperatures, the circuit is simulated with QCADesigner and the highest and lowest polarizations for every output are studied. For instance, at \( T = 1 \text{ K} \), the highest and lowest polarizations of output cell of flip-flop are \( 9.42 \text{ and } -9.42e^{-1} \), respectively. Therefore, the AOP for output cell Q is \((9.42e^{-1})–(–9.42e^{-1})/2 = 3.46\). Similarly, others AOPs for different cells of each layout at separate temperatures are estimated and presented in Figure 10.

5. Conclusion

This paper, an advanced and uncomplicated QCA layout of RS flip-flop is analyzed. The outlined circuit is confirmed with the QCADesigner and QCAPro tool. In contrast with the earlier study, the outcomes presented that proposed flip-flop is improved in terms of dimension, cell number, and delay. Moreover, the layout does not involve any rotated cells and it is efficient in terms of energy and reliability where the design have been permitted with QCADesigner. The proposed design present superior possibilities to significantly inflate the performance precisely for conceiving higher power-competent excessive efficiency circuit structures. Thus, this structure can be utilized to design circuits for nanocomputing and applying such competent circuit will absolutely be a revolution in the field of computation.

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