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ELECTRICAL & ELECTRONIC ENGINEERING | RESEARCH ARTICLE

Performance evaluation of efficient combinational logic design using nanomaterial electronics

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Abstract: Scaling down trend of CMOS transistor is approaching its lowest point, the rational substitute for the CMOS technology to attain advance improvements in terms of size, low power, and device density usage is an imperative essential. Due to the several physical limitations and circuit bounds of CMOS technology, it is the requirement of a new possible consistent model, that has small area, high device density and low power consumption. Quantum-dot Cellular Automata (QCA) is a novel approach in this direction. This paper presents a new design of 2:4 Decoder, 2:1 Multiplexer, D-Flipflop based on QCA. In addition, a nano communication circuit has been proposed which is proficient as compared to previous designs. Hamming distance approach has been used to perform the power calculations of the proposed circuits. To authenticate the functionality of the proposed designs computational simulation results has been performed using the QCAdesigner tool.

ABOUT THE AUTHORS

Md. Abdullah-Al-Shafi received his BSc (Engg.) in Information and Communication Technology in 2015. Currently pursuing an MS in Information Technology (IT) in Institute of Information Technology (IIT), University of Dhaka, Bangladesh. He has more than 15 research publications in renowned international journals and conference. His research area includes Distributed Computing, Quantum-dot Cellular Automation, Intelligent System and Wireless Sensor Network.
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PUBLIC INTEREST STATEMENT

Quantum-dot Cellular Automata is a unique computation methodology which is founded on semiconductor substantial. This standpoint article depicts four imperious circuit model of decoder, multiplexer, nano-communication circuit and reversible D flip-flop. The main meaning of the proposed layouts is designing without wire-crossing as well as consumed less number of QCA cell and area. Furthermore, the layouts are significantly lessened in terms of majority voters, cell intricacy, and latency. The proposed outlines achieved immense enhancement compared to earlier outlines. Power dissipation by the layouts indicates that all designs depleted extremely low energy. The multiplexer layout can be expended to realize complex communication system or computer memory, decoder can be used in memory system, chips and instruction decoding. The proposed nano-communication circuit can be used for protected communication.

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1. Introduction

CMOS technology has been emerged over the last four decades as a predominant technology of microelectronic. However, the concept of device scaling has made CMOS technology to the several physical limitations. Exports adored more speed and miniaturizations have brought down the planer device to the nanotechnology and quantum devices. Nanotechnology has attention the widespread explores to replace the estimated restrictions of planer CMOS (Compano, Molenkamp, & Paul, 2000). More's law predicts that the number of devices integrated on a chip will be doubled in every 18-month (Henderson, Johnson, Janulis, & Tougaw, 2004). As the manifested restrictions of this technology such as fault analysis complications, speed, oxide thickness, and extent overhead; the effective substitute for the CMOS has grown into an instant requirement. Quantum-dot Cellular Automata (Lent, Tougaw, Porod, & Bernstein, 1993) has currently been identified as one of the new alternative technologies with conceivable applications in nanocomputing (Arqub, Al-Smadi, Momani, & Hayat, 2016) for its specific speed, smaller space, and very low power utilization in different computational functions (Abdullah-Al-Shafi & Bahar, 2016a; Lent et al., 1993). Quantum dots are small nano metric size (2–10 nm) composed of semiconductor elements. Their small size denotes that electrons do not have to move as far as equated with higher particles, so electronic tools conceived by quantum dots can perform swifter (Abdullah-Al-Shafi, 2016a; Arqub, 2015; Bahar, Abdullah-Al-Shafi, & Bhuiyan, 2017). In existing centuries, circuit realization using QCA architectures have been obtained an immense deal of reflection because of notable logic functions such as competent full adders (Abdullah-Al-Shafi & Bahar, 2016b; Roohi, DeMara, & Khoshavi, 2015) and reversible logic circuits (Abdullah-Al-Shafi, 2016b, 2017; Abdullah-Al-Shafi & Bahar, 2016c; Islam, Shafi, & Bahar, 2015, 2016; Shafi, Bahar, & Islam, 2015). Complex circuits including multiplexers, decoders and row decoders have extensive appliances in digital circuit applications (Sen, Dutta, Goswami, & Sikdar, 2014; Sen & Goswami, 2015). Several attempts have been made in logic design to enhance the performance of the multiplexers (Askari, Taghizadeh, & Farhad, 2008; Hashemi, Azghadi, & Zakerolhosseini, 2008; Kim, Wu, & Karri, 2007; Mardiris & Karafyllidis, 2010; Mardiris, Mizas, Fragidis, & Chatzis, 2008; Roohi, Khademolhosseini, Sayedsalehi, & Navi, 2011; Sabbaghi-Nadooshan & Kianpour, 2013; Sen, Dutta, Saran, & Sikdar, 2012; Sen & Goswami, 2015; Sen, Nag, De, & Sikdar, 2015; Sen et al., 2014; Singh, Pandey, & Wairya, 2016; Teodósio & Sousa, 2007), decoders (Debnath, Das, De, & Sadhu, 2016; Kianpour & Sabbaghi-Nadooshan, 2011; Makanda & Jeon, 2014; Vetteth, Walus, Dimitrov, & Jullien, 2002; Zhou, Xia, Wang, Shi, & Liao, 2012) and nano-communication circuit (Das & De, 2016; Debnath, Das, & De, 2016; Silva, Sardinha, Vieira, Vieira, & Neto, 2015) using QCA technology. This study proposes the novel and competent QCA multiplexer, decoder, nano-communication circuit and a reversible D flip-flop using QCA technology. The proposed designed circuits are compared to previous outlines (Askari et al., 2008; Das & De, 2016; Debnath, Das, & De, 2016; Debnath, Das, De, & Sadhu, 2016; Hashemi et al., 2008; Kianpour & Sabbaghi-Nadooshan, 2011; Kim et al., 2007; Makanda & Jeon, 2014; Mardiris & Karafyllidis, 2010; Mardiris et al., 2008; Roohi et al., 2011; Sabbaghi-Nadooshan & Kianpour, 2013; Sen & Goswami, 2015; Sen et al., 2012, 2014, 2015; Silva et al., 2015; Singh et al., 2016; Teodósio & Sousa, 2007; Vetteth et al., 2002; Zhou et al., 2012) where the outcomes show that the proposed designs have the preeminent performance in contrast with the earlier outlines. This study is organized in six sections. Section 2 concisely explains foundations of the QCA nano-technology. The proposed circuits with QCA presentation is organized is Section 3. Section 4 presents simulation outcomes with detail comparison. Power estimation with circuit stability is specified in Section 5 and lastly, the conclusion is provided in Section 6.

2. Methodology

QCA provisions logic cases not as voltage phases but rather based on the point of separate electrons. The central features are QCA wire, inverter and majority gates.

2.1. QCA cell

Cells are the elementary entities of QCA based circuit and they are usually constituted of four quantum dots positioned at the corners of a square pattern. Each cell is charged with two supplementary electrons which channel from one low potential state to another across a high potential direction and a back plane voltage switches the cell occupancy. The electrons will be located in transversely to each other owing to reciprocal repulsive electrostatic power, possessing the utmost distance between them. A remote cell may be in one of two corresponding energy positions. These positions are called cell polarizations $P = +1.00$ and $P = -1.00$ as shown in Figure 1 (a) $p = 0$ denotes an unpolarized cell which covers no information. A cell polarization P is -1 if the electrons are involved the locus 2 and 4, in the same way, a cell polarization P is $+1$ if electrons are involved the position 1 and 3. The cell polarization equation (Lent et al., 1993) is presented below.

$$P = \frac{(\rho_2 + \rho_4) - (\rho_1 + \rho_3)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \qquad (1)$$

where, the charge at dot *i* denoted by ρ_i

Figure 1. QCA cell with diverse polarization (a), QCA 45° wire (b), 90 wire (c), Majority voter function as 2-input OR gate (d), 2-input AND gate (e), 5-input majority gate (f) and robust inverter (g).
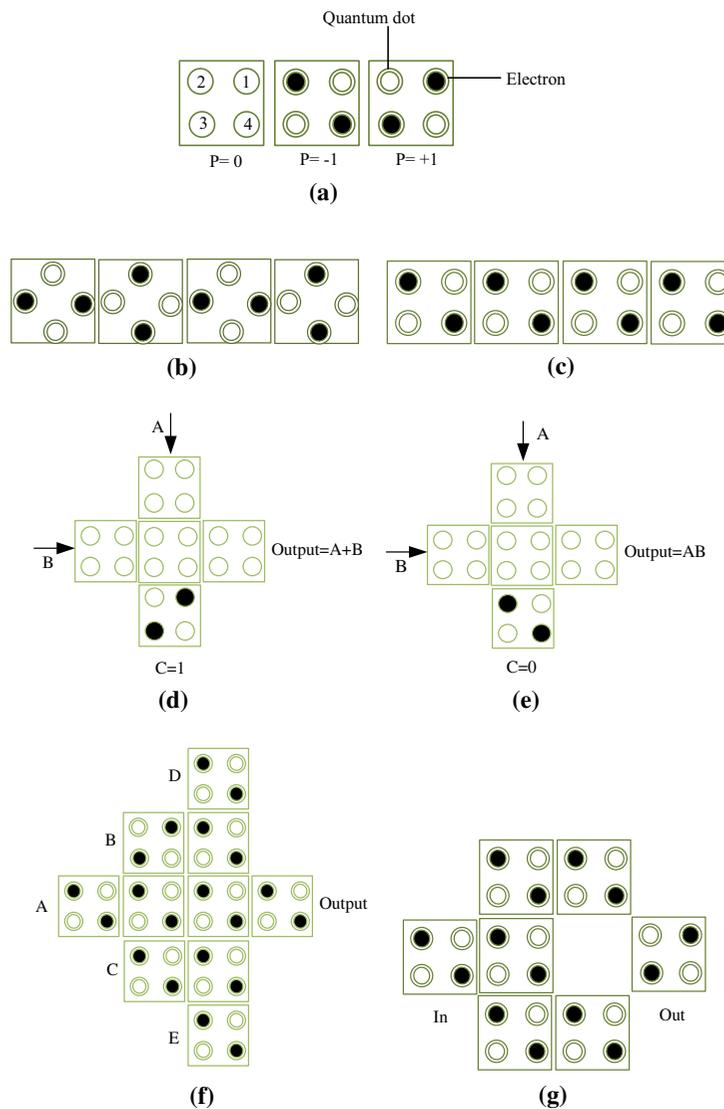
2.2. QCA wire

QCA wire encompasses of series of cells where the cells are united one after another (Abdullah-Al-Shafi, 2016a; Abu Arqub, 2015; Islam et al., 2016). QCA wire is employed to transfer signal from one position to another in a circuit. Logical charges are moved from cell to cell because of the coulomb contacts. There are two modes of alignments in a QCA wire namely binary wire and inverter chain. QCA wires can be either originated up of 45° cells or 90° cells as shown in Figure 1(b) and (c). In case of inverter, if two cells point at 45° with regard to each other their contact will be reverse and for that, these cells are mostly employed for coplanar wire crossings.

Binary wire transfers signal with similar polarity from one place to another, while inverter chain reverses the input cell polarity when odd figures of cells are employed in it.

2.3. Majority gates

Majority gate is assembled of five QCA cells; a central cell, one output, and three inputs. Polarity of the middle cell, as identified as device cell is imposed, by the coulomb repulsion to be equivalent to the output cell. The device cell at the center of the gate has its least energy when it accepts the polarization of the majority of the three input cells since this is the formation where the repulsion among the electrons in the three inputs cells and the electrons in the device cell is the lowest. So, an arrangement of inverter and majority voter is appropriate to construct an extensive logic set for scheming any circuit.

Majority voter can operate as AND or OR logic gate depending on the static polarity of the third input of the majority voter presented in Figure 1(d) and (e). Logical 2-input AND and 2-input OR functions can be executed using majority voter by putting one input cell to binary "0" and "1", subsequently. The logical equation of the 2-input majority gate can be stated as follows.

$$MV(A, B, C) = AB + BC + AC \tag{2}$$

The satisfying attainment of realizing a 3-input majority voter with five QCA cells inspired the analysts to hypothesize an inventive configuration for 5-input majority voter. Later, a specific layer (Abdullah-Al-Shafi & Bahar, 2016b) 5-input majority voter utilizing ten cells executed in a precise cell layout which is displays in Figure 1(f). The logic equation of the 5-input majority voter can be expressed as follows.

$$MV(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \tag{3}$$

2.4. QCA inverter

The inverter is a pattern of cells that reverse the input topology from one logic to another. Usually, two categories of inverter are applied (Abdullah-Al-Shafi, 2016b) that has been operated for the realization of several structures as an essential cell (Abdullah-Al-Shafi & Bahar, 2016c; Islam et al., 2015). The inverter can be designed by fixing QCA cells at 45° position (Abdullah-Al-Shafi & Bahar, 2016b) as appeared in Figure 1(g) which is potent and mostly used in circuit design. The logic values 0 and 1 transformed to 1 and 0 because of electrostatic repulsion.

2.5. QCA clocking mechanism

To form more complicated QCA devices, the location of QCA cell is not only essential also needs to coordinate the information, so that evade having a signal extending a logic gate and proliferating before the other inputs move the gate. This specific characteristic is particularly imperative in QCA circuits, ensuring its accurate function and this aspect are attained by QCA clock. The clock is an electrical region that switches the channeling barriers within a cell, therefore retaining control when a cell may or may not be polarized. QCA clocking is produced of four periods lagging by π/2 (Hennessy & Lent, 2001) as shown in Figure 2 which generates an innovative way to conceive nano-circuit distinct from the regular CMOS circuits (Walus, Dysart, Jullien, & Budiman, 2004). In each region, a certain potential can adjust the barriers between the dots and the organization of clock zones allows

Figure 2. QCA Four stage clocking (a) and signal for clocking zones (b).

(a)   (b)
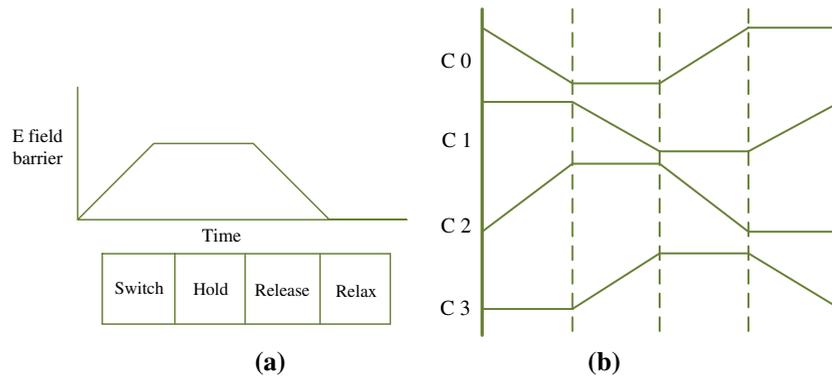
a group of QCA cells to construct a particular calculation and then its positions are stationary and its outputs can be applied as inputs to the following clock zone.

Switch period: the barrier between dots of QCA cell is elevated and the dots are motivated by the electron of its adjoining as well as electron begins channeling between dots. Thus, the cell turns into polarized.

Hold period: cell barrier stays high and electron cannot channel between dots and the cell keep its existing position.

Release period: barrier between dots are decreased, the electron can channel within dots and cell comes to be unpolarized.

Relax period: barrier remains at lowered and cell stays in unpolarized position.

3. Proposed QCA outlines

An assay is fulfilled to acquire the required devices and selected to realize the suggested design. The composition level is permitted applying a number of approximate simulators as the nonlinear approximation methods and bistable simulation device. However, these approximate do not develop the specified measures because these methods are iterative. In time, the QCA Designer is preferred simulation tool (Walus et al., 2004). The Bistable simulation tool has been occupied in the simulation interface between cells, clearly, the contact force linking two cells decomposes contrariwise with the fifth power of the length untangling them. During this estimation, not all the cells impact are counted and cell within the radius of R are being measured. For cell i, the scientific pattern is depicted by the following Hamiltonian.

$$H_i = \sum_j \begin{pmatrix} -\frac{1}{2}P_j E_{i,j}^k, & -\gamma \\ -\gamma & \frac{1}{2}P_j E_{i,j}^k \end{pmatrix} \tag{4}$$

where P_j is the polarization for cell j, $E_{i,j}^k$ is the k_{ink} energy between the cells (i and j) and γ is the channeling energy. For every cell i, the amount of the hamiltonian is over all cells (viz., j) in its radius of effect R. The Jacobi algorithm has been utilized to obtain the eigenvectors and eigenvalues of the Hamiltonian. At the layout level, small QCA block is designed and simulated for analysis its precision. Later these QCA blocks are unified together through QCA wire to manage the proposed composition. Finally, the consistency of the design is surveyed by the QCA Designer. The simulation outcome the essential waveform for the logical circuit and during simulation, it created few criterion that contains default standards as the cell size, layer separation, relative permittivity, samples number etc.

3.1. 2:4 decoder

The proposed 2:4 decoder uses four-periods clocking zones in QCA. The QCA layout of the proposed decoder circuit is shown in Figure 3(a) using four majority voters and three inverters. The logical expression of 2:4 decoder is described as. The input signals (X, Y) are decoded as:

$$R_3 = mv(X, Y, 0) = X \cdot Y \tag{5}$$

$$R_2 = mv\left(\overline{mv(X, Y, 0)}, 0, B\right) = \overline{X} \cdot Y \tag{6}$$

$$R_1 = mv\left(mv(X, Y, 1), \overline{Y}, 0\right) = X \cdot \overline{Y} \tag{7}$$

$$R_0 = \overline{mv(X, Y, 1)} = \overline{X} \cdot \overline{Y} \tag{8}$$

3.2. 2:1 Multiplexer

The proposed 2:1 multiplexer has two inputs in1 and in2, one address line s and single output state. If address line $s = 0$, input in1 is selected, and when $s = 1$, input in2 performs at the output. The majority voter illustration of the function is as followed.

$$mux = mv(mv(\overline{s}, in1, 0), mv(s, in2, 0), 1) = in1 \cdot \overline{s} + in2 \cdot s \tag{9}$$

Figure 3. QCA outline of proposed 2:4 decoder (a), 2:1 multiplexer (b), nano communication circuit (c) and D flip-flop (d).
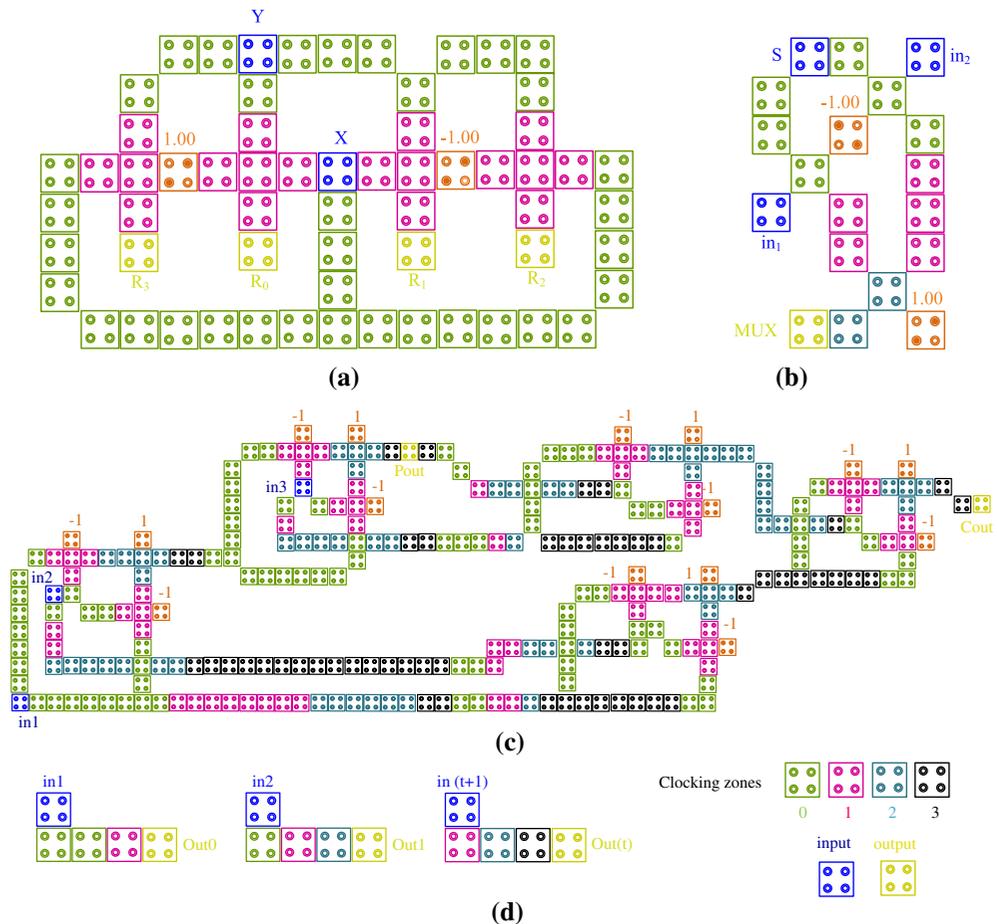
3.3. Nano communication circuit in QCA

The proposed complex circuit is designed using a parity checker and parity generator function. Parity initiator or generator selects bit data as an input signal and produces parity bit. Through transmission channel, the bit data and generated parity bit are directed to parity checker. Then the bits are verified by checker circuit which was covered within the message for fault detection. If the parity bit is not odd, then a fault is arises all through the transmission. The QCA layout of the proposed circuit is presented in Figure 3(c).

3.4. Reversible D flip-flop

The inputs of reversible D flip-flop is defined as in (t + 1), in2, in1 and the corresponding outputs lines are out (t), out, out1. The input arrangements from "000" to "111" allow one to one correlation with the outputs. The logical expression can be derived as in (t + 1) = out (t), in2 = out, and in1 = out1. The straight interactions between the output and input cells are presented in Figure 3(d). The proposed figure shows one to one correlation so only with certain delay, the inputs should shift the outputs unaffected.

4. Simulation results and performance analysis

Simulation results functionally have been obtained using the QCA Designer (Walus et al., 2004) that is a popular engine for QCA circuits. The simulation results of the proposed outlines are shown in Figure 4. The used criterions for the simulation are as follows: samples number: 12,800, convergence tolerance 0.001, radius of effect (bistable and coherence) 65 and 80 nm, threshold (lower and upper) −0.50 and 0.50, scale of cell is 18 nm, separation of layer is 11.50. The decoder circuit involves only 83 cells and covering an extent of 0.08 μm^2, the multiplexer involves of 18 cells and covering an extent of 0.02 μm^2, the flip-flop layout involves only 9 cells and covering an extent of 0.02 μm^2 and the nano communication circuit involves of 275 QCA cells with an extent of 0.41 μm^2. It is very essential to create an operationally firm layout in QCA and there are certain concerns realized into account to rise the design stability. When building models in QCA, a substantial attempt should be made to maintain the wire length in a specified clocking region to a minimum.

In Figure 4(a), the input X and Y to the output signals of R_3, R_2, R_1, R_0 in this unit goes through four clock levels, so the delay is an entire clock cycle. Hence the output, R_3, R_2, R_1, R_0 is presented single clock cycles after X and Y have been affected. The output value of R_0 is up when the input $X = Y = 0$ if the input is $X = Y = 0$ then the output value of R_1 is low. The starting position of the output line R_0 and R_1 is shown by arrows in the figure.

In the multiplexer outline, input in1, in2 and address line s is 01010101, 00110011 and 00001111 correspondingly. The result is 01010011 as presented in Figure 4(b). From the figure, it can be studied that for the primary four clock cycles address line is zero the output is following the input in1 for these four cycles, and when address line is 1 for succeeding four clock cycles, the result is following input in2.

Figure 4(c) explains the nano communication architecture, when the input bits to the transmitter are in1 = in2 = in3 = 0, then the corresponding output will be Pout = 1. In the recipient section, if the inputs are in1 = in2 = in3 = 0, the output will be Cout = 0. Similarly, others bit streams can be formed. The output Pout and Cout perform after the second cycle as indicated by arrows in the figure.

The outcome of proposed reversible D flip-flop is presented in figure 4(d) where the outputs out = out(1) = out(t) is low if all the inputs in1, in2 and in (t + 1) are low. Inputs are functional at "0" clocking region and outcome are gained at following clock zone so, the outcome is consistent and firm.

The layout intricacies in terms of the majority voters number, QCA cells, circuit thickness and the clocking zones applied to devise the circuits as presented in Table 1.

Figure 4. Simulation results of 2–4 decoder (a), 2-1 multiplexer (b), nano communication circuit (c) and D flip-flop (d).
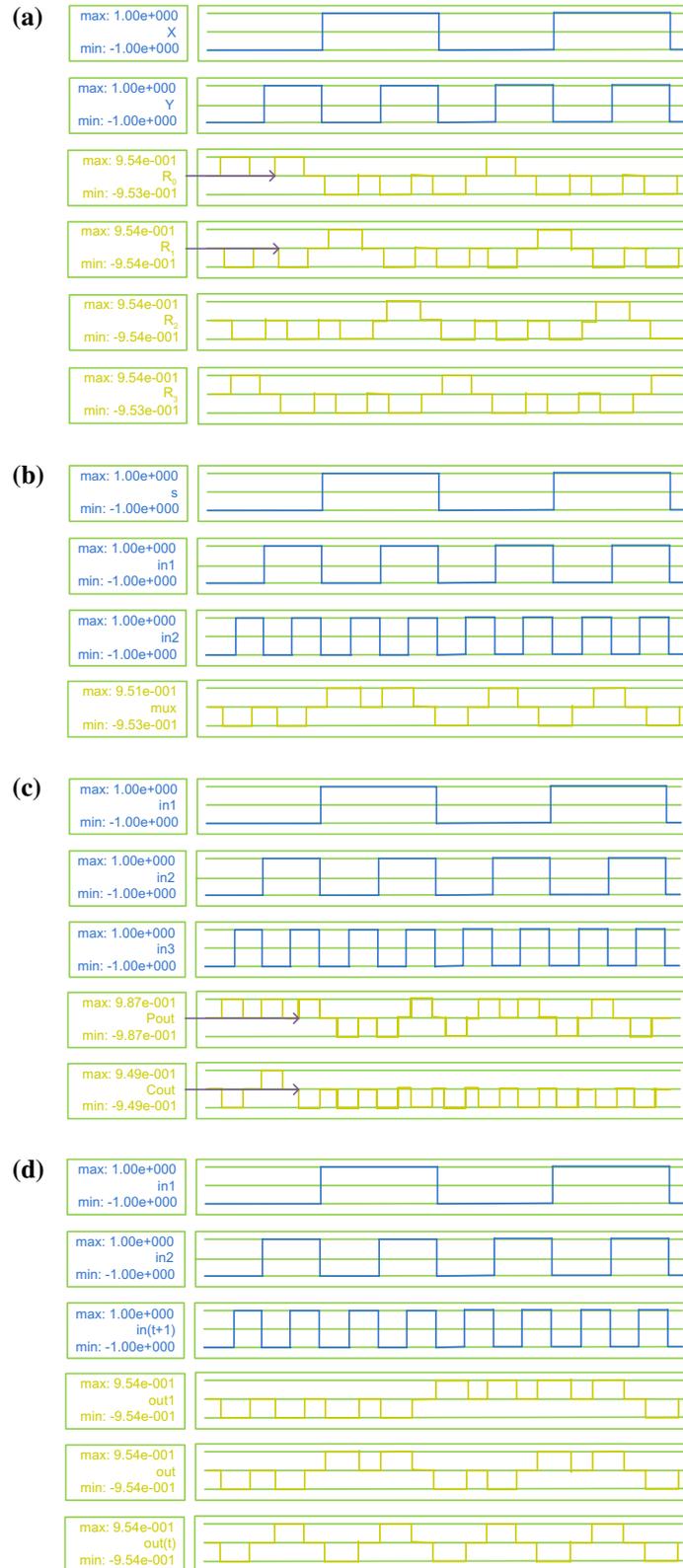
**Table 1. Complexity study of proposed circuits**

Outline	Majority voters	Cell used	Cell area (μm²)	Used area (μm²)	Clock used	Area usage (%)	Quantum cost
Decoder	4	62	0.020	0.050	3	40.00	0.050
Multiplexer	0	19	0.006	0.020	3	30.00	0.011
Nano. circuit	15	275	0.089	0.410	4	21.70	1.640
D flip-flop	0	10	0.003	0.010	3	30.00	0.005

Table 2. Performance analysis of proposed multiplexer with existing outlines

Multiplexer type	Outline	Cell intricacy	Used area (μm²)	Latency (clock cycle)
MUX 1	Outline in (Sen & Goswami, 2015)	23	0.02	2
MUX 2	Outline in (Sen et al., 2014)	19	0.02	2
MUX 3	Outline in (Sen et al., 2012)	19	0.02	3
MUX 4	Outline in (Sen et al., 2015)	23	0.01	2
MUX 5	Outline in (Teodósio & Sousa, 2007)	146	0.28	8
MUX 6	Outline in (Teodósio & Sousa, 2007)	88	0.14	4
MUX 7	Outline in (Sabbaghi-Nadooshan & Kianpour, 2013)	26	0.02	2
MUX 8	Outline in (Sabbaghi-Nadooshan & Kianpour, 2010)	56	0.07	4
MUX 9	Outline in (Hashemi et al., 2008)	36	0.06	4
MUX 10	Outline in (Kim et al., 2007)	46	0.08	4
MUX 11	Outline in Mardiris et al. (2008)	67	0.14	4
MUX 12	Outline in (Askari et al., 2008)	35	0.04	4
MUX 13	Outline in (Roohi et al., 2011)	27	0.03	3
MUX 14	Outline in (Singh et al., 2016)	19	0.02	1
Proposed outline		19	0.02	0.75

The designed multiplexer is compared with previous outlines in terms of area, cell number, and delay. The effects are presented in Table 2. The proposed circuit has 17.39 and 62.50% enhancement in terms of QCA cell and delay compared with (Sen & Goswami, 2015) and 29.63 and 75.00% enhancement in terms of cell and delay correspondingly, comparative to the outline proposed in (Roohi et al., 2011). Likewise, other enhancements are showed in Figure 5(a). The assessment in Table 2 presents that the proposed multiplexer outline has minimal cell count with better device thickness and is relatively faster than existing outlines.

Figure 5. A comparative study of proposed multiplexer (a), decoder (b) and nano communication circuit (c).
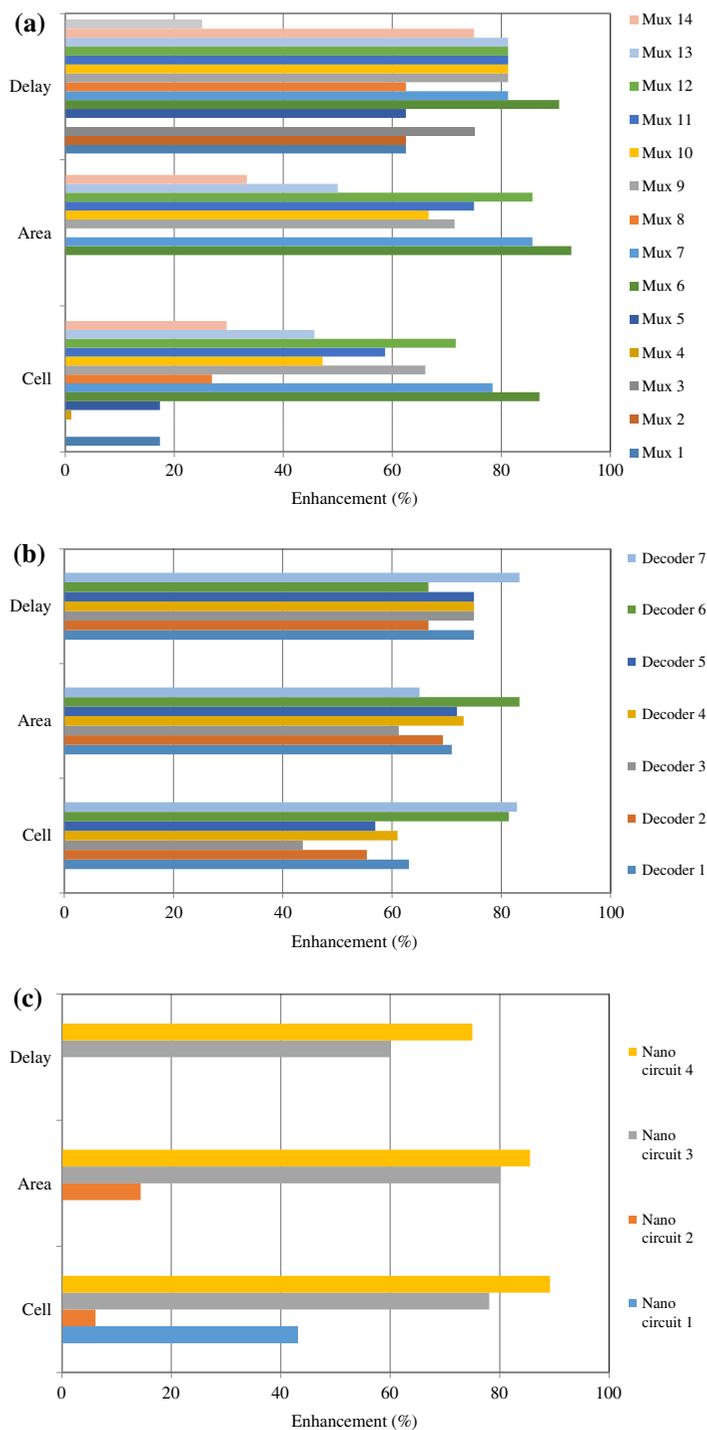
The decoder is assessed with previous outlines in terms of area, cell number and delay and the results are presented in Table 3. The proposed circuit has enhancements of 56.94, 71.91 and 75% in terms of cell, area and clock delay correspondingly, comparative to the outline proposed in (Vetteth et al., 2002). Likewise, other enhancements are showed in Figure 5(b). The assessment in Table 3 presents that the proposed decoder outline has better performance than existing outlines.

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Table 3. Performance analysis of proposed decoder with existing outlines				
Decoder type	**Outline**	**Cell intricacy**	**Used area (μm^2)**	**Latency (clock cycle)**
Decoder 1	Outline in (Zhou et al., 2012)	168	0.172	2
Decoder 2	Outline in (Zhou et al., 2012)	139	0.163	1.5
Decoder 3	Outline in (Makanda & Jeon, 2014)	110	0.129	2
Decoder 4	Outline in (Makanda & Jeon, 2014)	159	0.186	2
Decoder 5	Outline in (Vetteth et al., 2002)	144	0.178	2
Decoder 6	Outline in (Debnath et al., 2016)	333	0.300	1.5
Decoder 7	Outline in (Kianpour & Sabbaghi-Nadooshan, 2011)	362	0.143	3
Proposed outline		62	0.050	0.50

Table 4. Performance analysis of nano communication circuit with existing layouts				
Design	**Outline**	**Cell intricacy**	**Used area (μm^2)**	**Latency (clock cycle)**
Nano circuit 1	Outline in (Debnath et al., 2016)	483	0.335	0.75
Nano circuit 2	Outline in (Das & De, 2016)	293	0.479	2
Nano circuit 3	Outline in (Silva et al., 2015)	1255	2.064	5
Nano circuit 4	Outline in (Silva et al., 2015)	2544	2.838	8
Proposed layout		275	0.410	2

Table 4 presents the comparison study of the proposed nano communication circuit with existing designs. The circuit attains 6.14 and 14.40% improvements in terms of cell and area as compared with (Das & De, 2016) and other enhancements are illustrated in Figure 5(c).

The overall enhancements of proposed decoder, multiplexer, and nano communication circuit are demonstrated in Figure 5, correspondingly.

5. Power consumption of the proposed outlines

The dissipation of power by each QCA cell in a circuit is identical (Abdullah-Al-Shafi & Bahar, 2016b, 2016c). Therefore, in a range of connected QCA cells, the total dispelled power can be projected by adding the dispelled power of each cell within the range. The circuit's power consumption is reliant on the logic gates operated in constructing the circuit. Apply a larger quantity of logic gates, involves larger power dissipation by the circuits. The dispelled energy of the circuit is the total of the power dissipated by all the majority voters, inverters, and the range of QCA cells. This paper, mathematical

analysis of Hamming distance based assessment of power dissipation is applied to achieve the power dissipation of the proposed circuits. The assessment is achieved using the similar temperature (i.e. T = 2.0 K) and the similar channeling energies (i.e. $0.25E_k$, $0.75E_k$, etc.). It has been described (Liu et al., 2012) that for a shift in the Hamming distance between inputs to the circuit, the energy dispelled will also be differ.

In the case of the inverter, $1 \rightarrow 1$ or $0 \rightarrow 0$ input switching means Hamming distance "0", and the inverter has dispelled the power of 0.8 meV at $\gamma = 0.25E_k$ and 2.7 meV at $\gamma = 0.5E_k$. A ceiling Hamming distance of "3" is measured for the majority voter for $000 \rightarrow 111$ input switching, that affects the ceiling dissipated the energy of 41.0 meV by the majority voter at $\gamma = 0.25E_k$ and 41.2 meV at $\gamma = 0.5E_k$. Correspondingly, dissipation of power by the majority voter and inverter for several Hamming distances was testified in. The QCA design of the proposed decoder consists of three inverters and four majority gates. Each of these majority voters has one stable input polarization. Therefore, the Hamming distance for these majority voters is measured to be "2", respectively. For maximum energy dissipation, Hamming distance "1" is measured for each of the inverters. Applying the Hamming distances related to the input to logic gates and counting the QCA arrays perform in decoder as shown in Figure 3(a), the power dissipation of the proposed decoder is analyzed. The results are shown in Table 5. An equal method is applied for figuring the power dissipation by the multiplexer and nano communication circuit and the outcomes are denoted in Table 5. Table 5 illustrates that the power dissipated by the decoder at $\gamma = 0.25E_k$ is 156.4 meV and at $\gamma = 1.0E_k$, it is 206.8 meV. Similarly, dissipated power by the other outlines is formed which is presented in Table 5. These outcomes show that all the circuits dissipate very little heat energy. The results are also outlined in Figure 6.

Table 5. Power dissipation of the proposed circuits				
Outline	**Depletion at T = −271.15°C**			
	$\gamma = 0.25E_k$ (meV)	**$\gamma = 0.50E_k$ (meV)**	**$\gamma = 0.75E_k$ (meV)**	**$\gamma = 1.00E_k$ (meV)**
Multiplexer	94.3	101.8	108.3	116.6
Decoder	156.4	178.5	191.6	206.8
Nano. circuit	648.5	678.8	729.5	778.6

Figure 6. Power depletion of the proposed architecture.
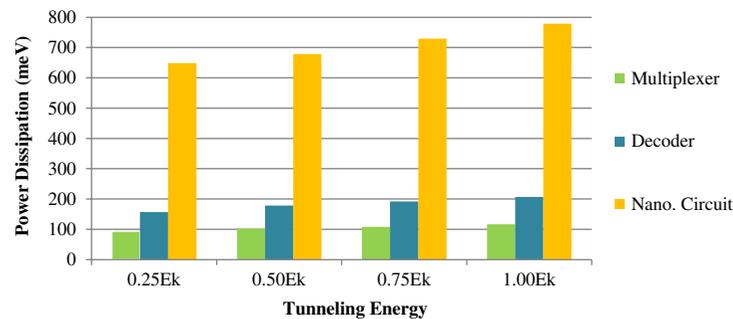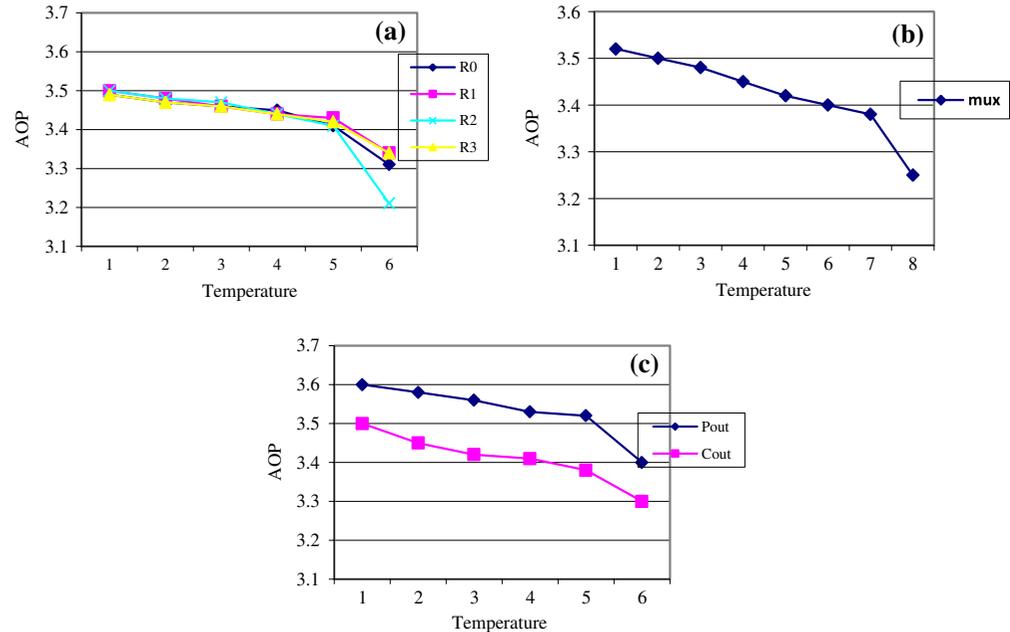
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Figure 7. Temperature effect on AOP of the proposed multiplexer (a), decoder (b) and nano communication circuit (c).

The average output polarization (AOP) of any cell of the QCA circuit is decreased by enhancing the temperature (Abdullah-Al-Shafi & Bahar, 2016b). The outcome of temperature on the AOP of the urged circuits is presented in Figure 7. The AOP of the output of the proposed decoder is slowly lessened, up to a temperature of T = 5 K. Multiplexer work competently between 1 and 7 K. Similarly, the nano communication circuit work proficiently between 1 and 5 K.

6. Conclusion

QCA is a new and ultra-high speed nanotechnology. In this paper, novel architecture of multiplexer, decoder, D flip-flop and nano-communication circuits have been proposed, which are faster and more efficient than existing layouts. The proposed QCA circuit's excelled the existing one in terms of cell complexity, area, wire crossing and latency. Moreover, the proposed circuits dissipate low heat, presents that the proposed QCA structures are appropriate for applying complex logic circuits. In future, the high robustness of reversible/ irreversible logic can be implemented using the proposed structures. These can be most commonly utilized to design faster, denser and fault-tolerant circuits.

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