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ELECTRICAL & ELECTRONIC ENGINEERING | RESEARCH ARTICLE

Optimized design and performance analysis of novel comparator and full adder in nanoscale

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Abstract: In a vastly rapid progress of very large scale integration (VLSI) archetype, it is the requirement of moment to attain a consistent model with swifter functioning speed and low power utilization. Quantum-dot Cellular Automata (QCA) is an inimitable transistorless computation approach that is based on semiconductor substantial and a substitute for customary CMOS and VLSI archetype at nanoscale point which comprises a better switching frequency, enhanced scale integration and small extent. In the design of digital logic, a comparator is the essential forming component which implements the resemblance of two numbers and a binary full adder is a major entity in digital logic systems. This paper deals with an expanded layout of reversible 1-bit comparator and proficient full adder without wire-crossing in QCA. The proposed layouts are significantly declined in terms of area and cell complexity, assessed to other layouts and clock cycle is retained at least. Quantum costs of the proposed circuits are estimated and compared, that shows the proposed QCA layouts have lesser quantum cost equated to regular designs and the energy depletion by the circuits endorses the view of QCA nano-circuit attending as a substitute level for the completion of reversible computing. Under thermal unpredictability, the constancy of the proposed designs is evaluated which show the operating efficacy of the designs. The simulation outcomes in QCADesigner tool approve that the presented designs performs properly and can be operated as an extreme performing design in QCA technology.

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PUBLIC INTEREST STATEMENT

Here has been cumulative concern in recent years that the limits of what can be attained with current approaches to improving device performance will soon be reached. Quantum-dot cellular automata (QCA) have been proposed as a means of getting around these limitations of CMOS technology. This standpoint article depicts two imperative QCA designs of comparator and full adder. The main significance of the proposed model is designing without wire-crossing where its top counterparts designed through wire crossing. Quantum cost of the proposed comparator is only five which is much reduced than existing and other proposed designs and attained 44.45% improvement compared to existing layout. Power dissipation analysis indicates that both design depleted extremely low energy.

Subjects: Computer Science; Engineering & Technology; Nanoscience & Nanotechnology

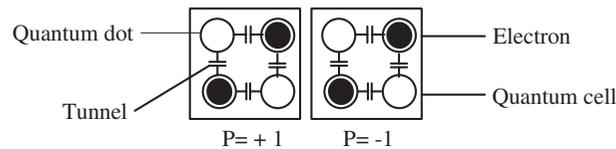
Keywords: quantum cellular automata; comparator; binary full adder; power consumption

1. Introduction

In the proximate future, it is predictable that the usual CMOS archetype extends to the culmination of its roadmap due to numerous thoughtful disputes as impurity discrepancies, elevated outlay of lithography and more notably (Lent, Tougaw, Porod, & Bernstein, 1993; Tóth & Lent, 1999; Wilson, Kannangara Geoff Smith, Simmons, Raguse, & Raguse, 2002). Various technological prototype for instance Resonant Tunneling Diode, Field Effect Transistor (FET) based on Carbon Nanotube and Quantum-dot Cellular Automata have been come out to explain the revealed complications (Amlani et al., 2000; Rumi, Walus, Wang, & Jullien, 2004). As per the international technology roadmap for semiconductors (ITRS) statement that proposes a precise brief of potential archetypes, QCA is one of the pledging upcoming solutions (The International Technology Roadmap for Semiconductors, 2001) and in recent times has been accepted as one of the eminent six evolving archetypes with potential utilizations in forthcoming computing. QCA prototype is centered on a precise primitive fact, termed coulomb repulsion that utilizes position of electron sets rather than voltage points for logical approaches. The data is embodied by polarizations of the cell, which are organized by inputs and clock phases (Tougaw & Lent, 1994; Tougaw, Lent, & Porod, 1993). A main improvement of QCA nano-device is the simple interconnection that is feasible with this archetype. As the cells connect merely with their adjacent neighbors, there is no necessity for extensive interrelation lines. Separate phases like algorithmic and material based models are analyzed in QCA. In top level outlines, consideration is on the algorithmic and rational outline along with the material outline. Though, physical connections can be problematic in device operation and organize of the physical connections is an obligatory difficulty in the actual QCA circuit outlines, particularly in outsized systems (Cho & Swartzlander, 2007). The QCA circuits have been formed and enhanced in the terms of area, complexity, and latency (Abdullah-Al-Shafi & Bahar, 2016a; Al Shafi, Bahar, & Islam, 2015; Al-Shafi, 2016). Several logical designs as adders (Cho & Swartzlander, 2005; Hashemi, Tehrani, & Navi, 2012; Navi, Farazkish, Sayedsalehi, & Rahimi Azghadi, 2010; Rumi et al., 2004; Shams & Bayoumi, 2000; Vetteth, Walus, Dimitrov, & Jullien, 2002) and sequential circuits (Kummamuru et al., 2003; Momenzadeh, Huang, & Lombardi, 2005; Niemier & Kogge, 2001; Walus, Jullien, & Dimitrov, 2003; Yang, Cai, Zhao, & Zhang, 2010) are applied in QCA archetype. This paper proposed a new QCA comparator and full adder layout in single layer which is enriched in term of cell and area complexity in contrast to other designs (Abedi, Jaberipur, & Sangsefidi, 2015; Angizi, Alkaldy, Bagherzadeh, & Navi, 2014; Basha & Kumar, 2012; Cho, 2006; Cho & Swartzlander, 2009; Das & De, 2015; Dehghan, Roozbeh, & Zare, 2014; Hänninen & Takala, 2010; Hashemi & Navi, 2015; Kianpour, Sabbaghi-Nadooshan, & Navi, 2014; Kim, Wu, & Karri, 2007; Navi et al., 2010; Pudi & Sridharan, 2012; Vetteth et al., 2002). The quantum costs and power depletion by the proposed designs are assessed besides constancy of the circuits under thermal roughness is evaluated in this paper. The outcomes of the simulation are verified with abstract values, indicating the exactness of the proposed circuits.

This article is prepared as follows. A concise explanation of QCA structure is explored in Section 2. The proposed circuits and their QCA designs are organized in Section 3. Section 4 deals with simulation outcomes, comparisons and discussions. The energy dissipation and constancy of the proposed designs under thermal roughness are explained in Section 5. Finally, in Section 6 the conclusion with future work of this article is drawn.

Figure 1. Structure of QCA cells.



2. Methods and materials

Quantum-dot cellular automata is a recent device outline that is suitable for the micrometer scale. This section, specific supportive background resources in appreciation the rest of this paper are presented.

2.1. QCA architecture

QCA is founded on the contact of bi-stable cells composed from four quantum dots. A top-stage outline of two polarized cells is displayed in Figure 1. All cells are composed from four quantum dots organized in a square outline (Tougaw & Lent, 1994; Tougaw et al., 1993). The cell is incited with two electrons, which are able to tunnel between neighboring quantum dots. The electrons be liable to engage antipodal positions accordingly of their reciprocal electrostatic revulsion. Hence, there remain two equally dynamically marginal compositions of the two electrons in the cell. These configurations are expressed as cell polarization $P = -1$ and $P = +1$ individually. Binary information can be encoded by applying polarization $P = -1$ to characterize logic “0” and $P = +1$ to characterize logic “1”.

The binary data is transferred from one input position to output position in a wire due to the coulombic interfaces between QCA cells (Abdullah-Al-Shafi, Shifatul, & Bahar, 2015; Al-Shafi, 2016). This is an effect of the structure trying to resolve to a ground status. Whichever cells alongside the wire that is anti-polarized to the input site would be at an upper energy stage and would shortly resolve to the precise ground status. The conduction in a 90° wire is presented in Figure 2(a). Except the 90° wire, a 45° wire can also be applied as displayed in Figure 2(b). In this perspective, the conduction of the binary data rotates between the two polarizations. Besides, there is an ostensible non-linear wire, where cells with 90° direction can be sited next to one another, except off center.

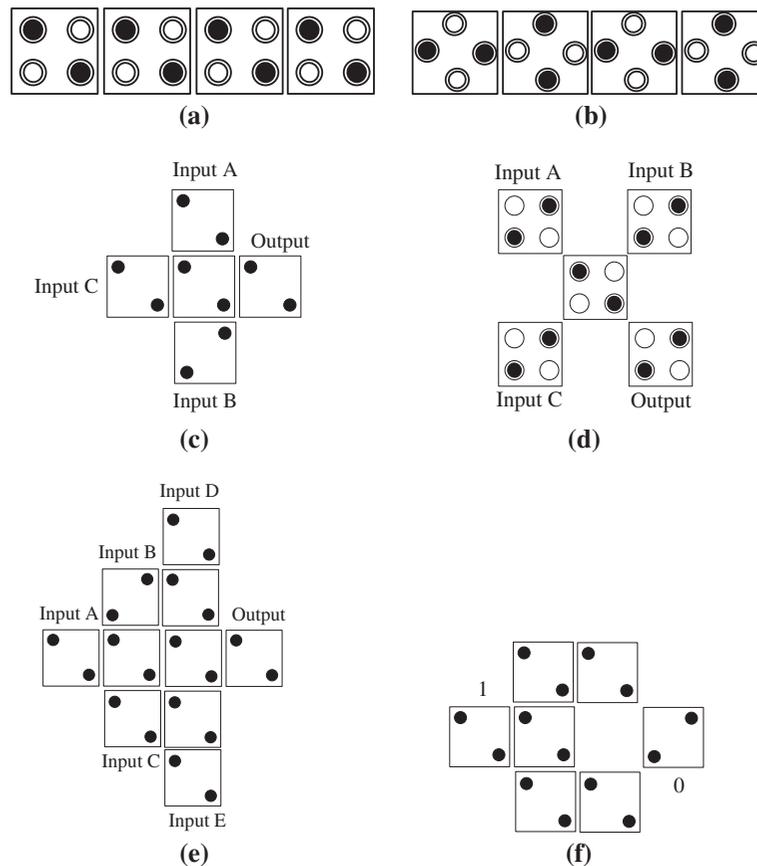
The majority voter acts a three pins logic function (Islam, Shafi, & Bahar, 2016). If the inputs are A, B and C then the function of the majority voter is,

$$m(A, B, C) = A \cdot B + B \cdot C + C \cdot A \quad (1)$$

By arranging the polarization of one input as logic “0” or “1”, an AND gate and OR gate can be realized correspondingly (Abdullah-Al-Shafi, 2016; Islam, Shafi, & Bahar, 2015). More complicated circuits can be assembled from AND gate and OR gate. Two forms of majority gate are shown in Figure 2(c) and (d), separately which are rotated and Original majority gate. Because of electrostatic revulsion among the electrons of the cells, the inner cells of both majority voters influence the outcome to the durable polarization. A five input majority voter consist of five inputs and one output cell. The inputs cell named A, B, C, D and E and the output cell is disclosed by output as presented in Figure 2(e). The input cells have static polarization however, output and central cells are allowed to alteration. Because of the effects among input and central cells, the majority result of inputs is moved to the output and forms the five input majority voter, proficiently.

QCA inverter is another construction part which has several outlines in QCA circuit design (Abdullah-Al-Shafi, 2016; Amlani et al., 2000; Lent et al., 1993). As per the coulomb revulsion, the smallest energy level for two transversely neighboring cells is when they hold reverse polarities. The inverter gate in Figure 2(f) breakups the input into double channels and it unites them by leveraging a 45° wire that generates the opposite polarization.

Figure 2. QCA Structure blocks; binary wires (a) 90°, (b) 45°, majority voter, (c) Original, (d) Rotated, (e) five input majority voter gate, (f) inverter gate.



For identification of the circuit effectiveness, specifically when the input move to the object statuses, the clocking signal procedure is utilized (Abdullah-Al-Shafi & Bahar, 2016a). As the entries of the majority voter that the values have to move at the uniform period into them. Usually QCA cells are separated to four time sections, in the signal clocking. Every sections, also named clock zone, supplements to one of the four segments: switch, hold, release and relax as showed in Figure 3. Interdot blocks are let down and transmission of data follows through electron channeling, throughout the switch level. The cells become polarized by steadily lifting the barriers. The barriers are sustained top in the hold level so the cell upholds the polarization and the outcome can be applied as inputs to the later segment. The cells begin to drop their polarization by declining the barriers throughout the release and relax levels and next they keep at in an unpolarized status. The power depletion of QCA is minimal as just two electrons are affecting. Maximum of the power needed by circuits will be consumed by the clocking mechanism (Vetteth et al., 2002).

Figure 3. Four phase clocking mechanism in QCA.

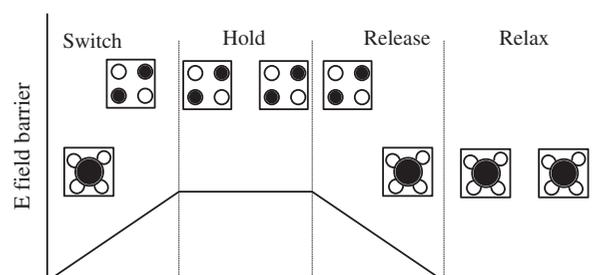
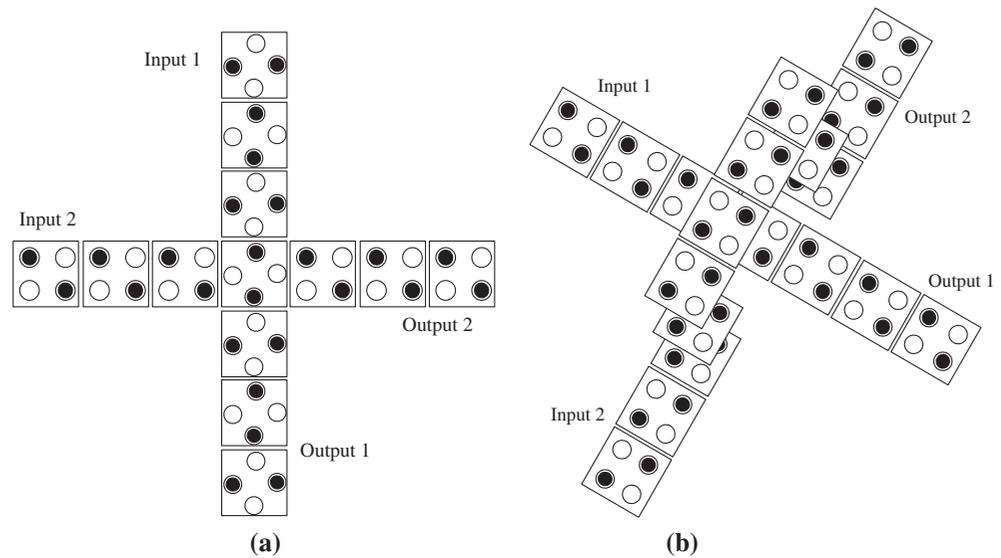


Figure 4. QCA crossing over
(a) coplanar crossing;
(b) multilayer crossing.



2.2. QCA crossing over

Two special arrangements of crossover are existing in QCA circuit design. The coplanar and multilayer crossovers are presented in Figure 4(a) and (b) individually. As illustrated in Figure 4(a), two separate signals in a coplanar outline can individually be transferred, because of hardly communication between normal and rotated cells when the two are positioned next to each other. Meanwhile this layout has few complications like crosstalk, other approaches have to be applied for resolving such complications. In the multilayer approach the signal permits through the higher level which some extends profits like tolerance to cell movement deficits and decreased extent occupation, presented in Figure 4(b). The multilayer crossover is required three layers for implementation as per coulomb repulsion.

3. QCA comparator and full adder design

Comparator can be described as a combinational circuit which completes the assessment of two numbers and defines if one of them is identical to, bigger than, or less than another number. The procedure is comparable to deduct micro-operation, distant from that the variation is not transferred to a focus register; just the status bits are influenced. If the numbers are A and B, then the result is stated by $A = B$, $A > B$, or $A < B$ as presented in Figure 5(a) and can be marked as follows. The mathematical table is presented in Table 1.

$$F_{(A>B)} = A'B = X \tag{2}$$

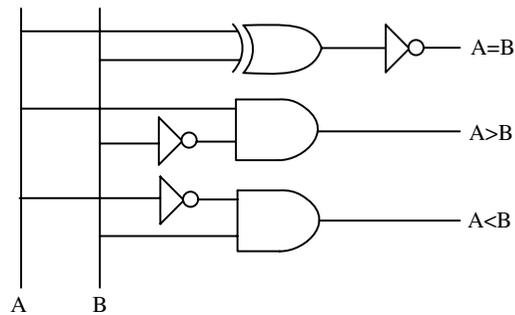
$$F_{(A=B)} = (A'B + AB')' = Y \tag{3}$$

$$F_{(A<B)} = AB' = Z \tag{4}$$

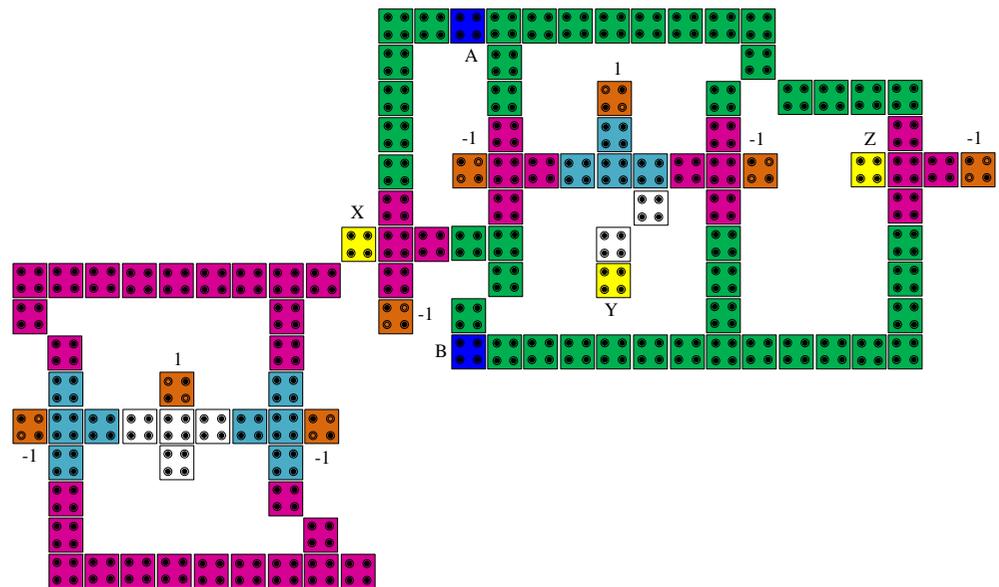
Table 1. Truth table of comparator

Input		Output		
A	B	X	Y	Z
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Figure 5. Proposed 1-bit comparator (a) logic circuit; (b) QCA design.



(a)



(b)

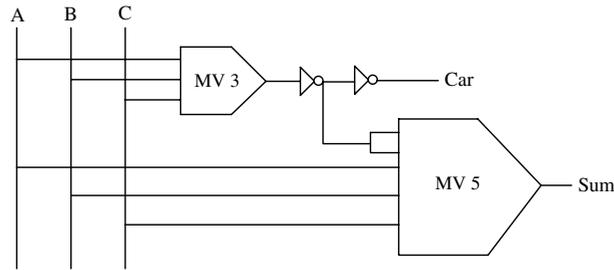
By joining the operational variety of Feynman and TR logic gate, the reversible comparator can simply be realized as presented in Figure 5(b). Single Feynman and TR circuit are needed to outline the 1-bit comparator. The outline constructs three succeeding outputs. The proposed comparator is design using regular cells and without wire crossing. It takes 117 cells and four clock levels to form precise results. In contrast to earlier outline the proposed comparator resulted in major changes in terms of cell and area complexity, and has a moderated quantum cost.

Binary accumulation is the very basic arithmetical process. Other computer mathematical strategies as multiplication and deduction are frequently performed by adders and the significance has encouraged different outlines for binary adder arrangements (Angizi et al., 2014; Bahar & Waheed, 2016; Cho & Swartzlander, 2009; Navi, Roohi, & Sayedsalehi, 2013; Navi, Sayedsalehi, Farazkish, & Azghadi, 2010; Rahimi Azghadi, Kavehei, & Navi, 2007; Roohi, Khademolhosseini, Sayedsalehi, & Navi, 2014; Sayedsalehi, Moaiyeri, & Navi, 2011; Wei Wang, Walus, & Jullien, 2003). The logical meanings of the adder can be stated as follows.

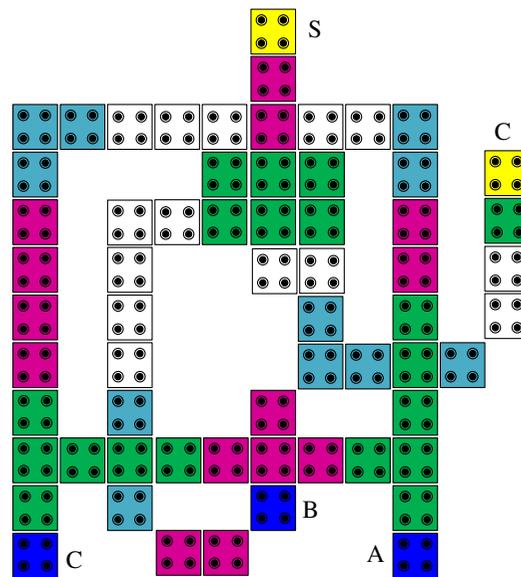
$$\text{Sum}(S) = A \oplus B \oplus C \tag{5}$$

$$\text{Carry}(C) = AB + BC + AC \tag{6}$$

Figure 6. Proposed full adder (a) QCA schematic; (b) QCA outline.



(a)



(b)

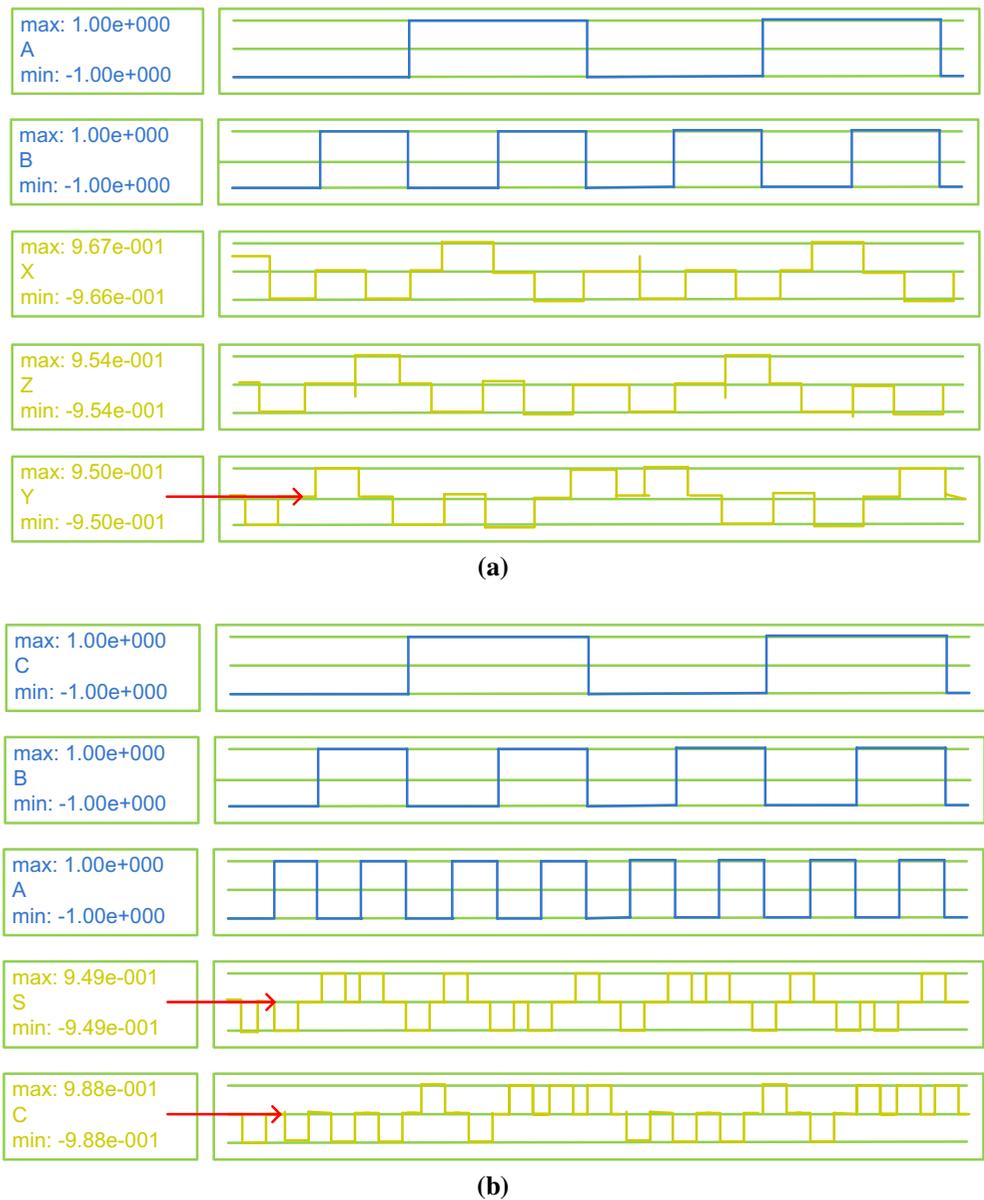
The designed binary full adder is carry out in single layer and only 63 cells with four clock levels is used to produce accurate outputs shown in Figure 6. In contrast to previous model the designed adder developed in considerable progresses in terms of area and cell complexity, wire crossing, and has an identical organization in terms of clock delay. Simulation outcomes part compares all earlier outlines and displays the achievement of the proposed layouts.

4. Simulation and experimental results analysis

The simulation are attained employing a recent specific-resolution tool, QCADesigner (Walus, Dysart, Jullien, & Budiman, 2004) ver. 2.0.3. The list of features applied for bistable and coherence vector simulation is presented as follows where most of the features are stable in QCADesigner. The dimension of the quantum cell is 18x18 and diameter 5 nm, 0.0001 convergence tolerance, 65.00 nm radius force, 9.800e22 clock high-level, 3.800e23 clock low-level, 100 highest iterations per sample, 1.00e016 time phase, 7.00e011 complete simulation period, 2.00 amplitude factor and 11.50 layer division.

Figure 7 presents the simulation results of comparator and full adder finalized in QCA and the outcomes are confirmed with abstract knowledge. For comparator if inputs A and B are both zero, then the output values for X, Z and Y are 0, 0, and 1, respectively. Similarly, for full adder if the input points are A = C = 0 and B = 1, then the outcomes are sum = 1 and carry = 0, correspondingly. The red arrow in output Y, Figure 7(a) define the initial point which is one clock level delay for output bits. In Figure 7(b), the red arrow denotes the initial point of output S and C.

Figure 7. Simulation outcomes for proposed QCA (a) comparator; (b) full adder.



4.1. Complexity of the proposed QCA comparator

Table 2 expresses the design complexity of the proposed comparator. The design is realized with eight majority voters, 117 cells with area of 0.18 μm^2 , and four clocking phases which is considerably better than earlier layout. The proposed comparator has cell improvement of 63.32% and area improvement of 47.52%.

Table 2. Complexity analysis of proposed comparator

Design	Majority voters	Cell used	Overall area (μm^2)	Cell area (μm^2)	Area usage (%)	Latency	Quantum cost
Proposed 1-bit comparator	8	117	0.182	0.037	20.56	2	0.720
Existing (Das & De, 2015)	17	319	0.343	0.103	30.15	3	3.087

4.2. Quantum cost of the proposed comparator

The cost of the logic circuit can be achieved by total number of AND, NOT, and XOR operation. The proposed 1-bit comparator design as indicated in Figure 5(b) needed only one Feynman and one TR gate. Therefore, the comparator has circuit cost as $(1 \times 4 + 1 = 5)$ as presented in Table 3. The compatible quantum cost of the proposed comparator is evaluated in Table 2. The proposed 1-bit comparator has 44.45% improvement in terms of quantum cost compared to existing design. The design has 61.54 and 54.55% development in terms of quantum cost over present NEW gate and DG gate based comparator (Dehghan et al., 2014), correspondingly. Equally the proposed comparator has improvement over Toffoli, Peres and Fredkin gate based comparator (Basha & Kumar, 2012). The general estimation is presented in Table 3.

4.3. Complexity of the proposed QCA full adder

Table 4 presents the layout complexity of the proposed single layer binary full adder. The design is achieved with single five-input majority voter, 63 cells with area of $0.05 \mu\text{m}^2$, and four phases of clock which is significantly worthier than earlier designs.

4.4. Comparison results among QCA full adders

An assessment between the proposed full adder and existing full adder outlines studied in this paper is achieved to analyze the formations of proposed QCA full adder. Table 5 synopsis that proposed design has meaningful enhancements in terms of area and cell complexity with clock delay retained at the minimum level in contrast to the earlier designs. A relative analysis of proposed binary full adder with previous outlines is shown in Figure 8.

As per Figure 8, the proposed full adder directs to about 78.42% enhancement in cell and 91.94% enhancement in area complexity in contrast to the full adder outline generated with inverters and three-input majority voters in (Vetteth et al., 2002). In similar way, other improvements are shown in Figure 8.

Table 3. Comparison among proposed comparator with the previous design

Design	Quantum cost	Improvement (%)
Proposed comparator	5	44.45
Existing comparator (Das & De, 2015)	9	
Peres gate based comparator (Basha & Kumar, 2012)	10	50
DG gate based comparator (Dehghan et al., 2014)	11	54.55
NEW gate based comparator (Dehghan et al., 2014)	13	61.54
Toffoli gate based comparator (Basha & Kumar, 2012)	16	68.75
Fredkin gate based comparator (Basha & Kumar, 2012)	23	78.26

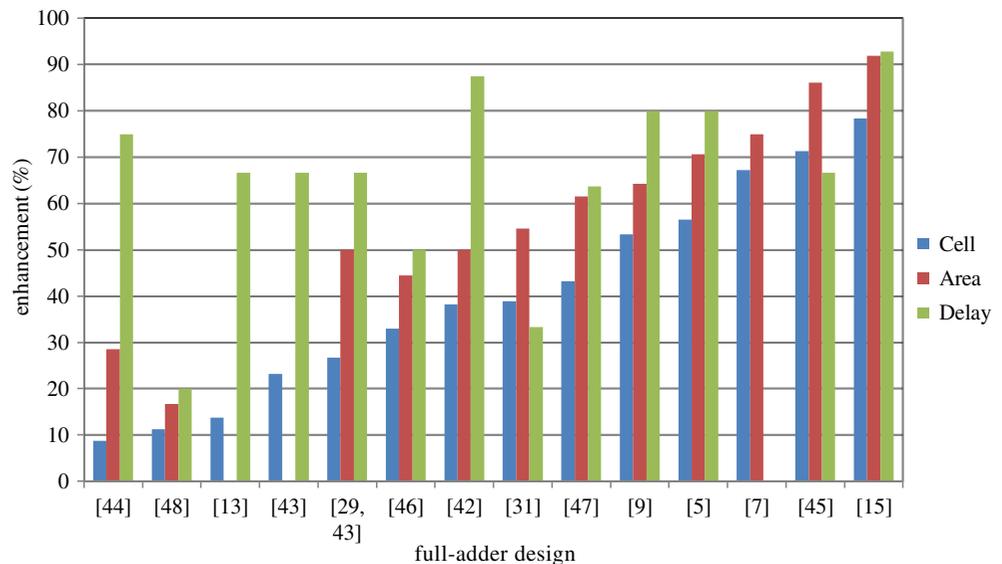
Table 4. Complexity analysis of proposed binary full adder

Design	Cell used	Overall area (μm^2)	Cell area (μm^2)	Area usage (%)	Latency	Quantum cost
Proposed full adder	63	0.05	0.020	40	1	0.05

Table 5. Comparison between proposed full adder with the existing designs

QCA layout	Cell complexity	Area (μm^2)	Clock cycle
Proposed layout	63	0.05	1
Layout in Kianpour et al. (2014)	69	0.07	4
Layout in Hashemi and Navi (2015)	71	0.06	1.25
Layout in Navi et al. (2010)	73	0.04	3
Layout in Cho (2006)	82	0.03	3
Layout in Cho (2006), Cho and Swartzlander (2009)	86	0.10	3
Layout in Pudi and Sridharan (2012)	94	0.09	2
Layout in Hänninen and Takala (2010)	102	0.10	8
Layout in Angizi et al. (2014)	103	0.11	1.5
Layout in Abedi et al. (2015)	111	0.13	2.75
Layout in Cho and Swartzlander (2007)	135	0.14	5
Layout in Rumi et al. (2004)	145	0.17	5
Layout in Tougaw and Lent (1994)	192	0.20	Not applicable
Layout in Kim et al. (2007)	220	0.36	3
Layout in Vetteth et al. (2002)	292	0.62	14

Figure 8. A relative analysis of proposed QCA full adder with earlier.



5. Power consumption and consistency of proposed QCA layouts

The power depletes from a particular cell rest on the level of transform of the clock and the channeling energy (Abdullah-Al-Shafi & Bahar, 2016b). The depleted power of a QCA outline in a particular clock level can be analyzed by totaling the power depleted by every inverter and majority voter (Liu, Srivastava, Lu, O'Neill, & Swartzlander, 2012). Power depletion of a circuit can be measured by Hamming distance.

For an inverter if the input pin is altered from $0 \rightarrow 0$ to $1 \rightarrow 1$, then Hamming distance will be zero, and the dissipation by inverter at $T = 2.0 \text{ K}$ and $\gamma = 0.25 E_k$ is 0.8 meV while for $\gamma = 1.0 E_k$, it will be 8.0 meV (Liu et al., 2012). For majority voter, dissipation is least, while the inputs are altered from $000 \rightarrow 000$ that is Hamming distance is zero, and the dissipation is top while polarization of all inputs are altered that is input polarization are altered from $000 \rightarrow 111$, Hamming distance is three. The

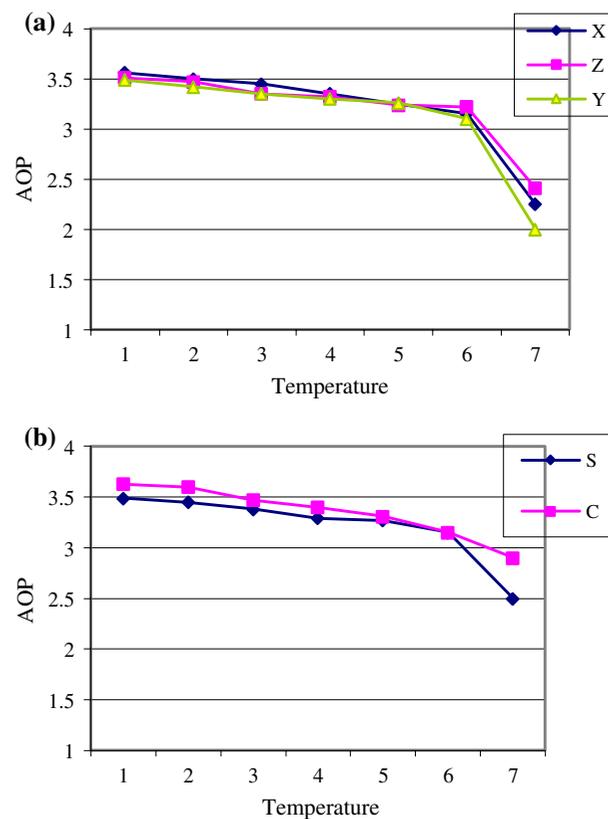
Table 6. Power dissipated by the proposed QCA circuits

Design	Energy dissipation at $T = 2\text{ K}$			
	$\gamma = 0.25 (E_k)$	$\gamma = 0.50 (E_k)$	$\gamma = 0.75 (E_k)$	$\gamma = 1.0 (E_k)$
1-bit comparator	352.8	380.8	396.8	415.6
Full adder	78.1	80.6	83.6	87.2

method reported in (Liu et al., 2012) is applied to result the dissipation of the proposed circuits at temperature $T = 2.0\text{ K}$ in separate channeling energy. The power depleted by the proposed circuits are summarized in Table 6.

The temperature impact on the output polarization of proposed comparator and full adder are performed. The output polarization is captured at several temperature with QCADesigner engine. The average output polarization (AOP) for every cell is analyzed from (Pudi & Sridharan, 2011) and presented in Figure 9. The designs performs proficiently in temperature scale of 1–6 K, and the AOP for every cell is altered very slight in this scale.

Figure 9. Temperature consequence on AOP of proposed (a) comparator; (b) full adder.



6. Conclusion

Conceiving a durable and single layer QCA comparator and full-adder is of immense significance to construct arithmetic circuit design. This paper, a stable comparator and full-adder is proposed and both the designs are without any wire crossing. Besides the calculation of power dissipation, quantum cost, and constancy analysis by the proposed layouts shows that the comparator and full-adder is extremely power effective circuit. Comparison outcomes show that these designs transcends its top counterparts in terms of area, cost, complexity, and delay and can be an appropriate element for recognizing logical QCA circuits. In future, the proposed binary full adder can be designed to implement advanced QCA adders and the comparator can be applied to realize complicated reversible circuit as n-bit comparator at nanoscale with minimum heat depletion.

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